Form PTO-1449 (Rev. 8-88) U.S. Department of Commerce Patent and Trademark Office INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) **Sheet 1 of 1**	Attorney Docket No.: 0321.67590	Serial No.: 10/526,523
	Applicant: Cheng	
	Filing Date: March 1, 2005	Group: 2818

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	1	International Technology Roadmap for Semiconductors: 2001 Edition – Interconnect (22 pp).
	2	Betz, V. and Rose, J., "Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency," in IEEE Trans. On VLSI, 6(3), pp. 445-456 (September 1995).
	3	Chen, H., Yao, B., Zhou, F. and Cheng, C., "The Y-Architecture: Yet Another On-Chip Interconnect Solution," Proc. of the Asia South Pacific Design Automation Conference, pp. 840-846, 2003.
	4	Cheng, E., Zhou, F., Yao, B., Cheng, C., and Graham, R., "Balancing the Interconnect Topology for Arrays of Processors between Cost and Power," International Conference in Computer Design, Freiburg, Germany (September 2002).
	5	Dally, W. and Towles, B., "Route Packets, Not Wires: On-Chip Interconnection Networks," IEEE Proc. of the 38th Design Automation Conf. pp. 684-689, 2001.
	6	Garg, N. and Konemann, J., "Faster and Simpler Algorithms for Multicommodity Flow and other Fractional Packing Problems," In Proc. of the 39th Annual Symposium on Foundations of Computer Science, pp. 300-309, 1998.
	7	Igarashi, M., Mitsuhashi, T., Le, A., Kazi, S. Lin, Y., Fujimura, A. and Teig, S., "A Diagonal-Interconnect Architecture and Its Application in RISC Core Design," 2002 IEE International Solid-State Circuits Conference, Session 12/TD: Digital Directions/12.8.
	8	Karmarkar, N., "A New Polynomial-time Algorithm for Linear Programming." Combinatorica, 4(4), pp. 373-395, 1984.
	9	Khalid, M. and Rose, J.,"Experimental Evaluation of Mesh and Partial Crossbar Routing Architectures for Multi-FPGA Systems," in IFIP IWLAS '97, Grenoble, France, pp. 119-127 (December 1997).
	10	Leiserson, C., "Fat Trees: Universal Networks for Hardware – Efficient Supercomputing," IEEE Trans. On Computers, Vol. C-34, No. 10, pp. 892-901 (October 1985).

Examiner	Date Considered

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.